CLAIM SET AS AMENDED

1. (Previously Presented) A liquid crystal display device comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a sealant between the upper and lower substrates in an area near an edge of the upper substrate;

a plurality of source and gate pads on the lower substrate;

a plurality of gate and data lines on the lower substrate, each gate line being electrically connected with the corresponding gate pad, each data line being electrically connected with the corresponding source pad;

a gate insulating layer between the gate lines and the data lines;

a source PCB and a gate PCB electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed along a first side and a second side, respectively, of the lower substrate and outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB, wherein the first and second sides meet at a corner of the lower substrate; and

a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB in

the vicinity of the corner of the lower substrate, wherein the plurality of transmitting wires are formed in a curved shape on the lower substrate from the gate pads to the source pads.

2. (Original) The device of claim 1, further comprising a plurality of switching devices.

3. (Currently Amended) The device of claim 1, wherein the ~~gate~~ transmitting wires include at least eight electrical wires.

4. (Original) The device of claim 1, further comprising a plurality of dummy pads between the adjacent gate pads and between the adjacent source pads.

5. (Previously Presented) A liquid crystal display device comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a sealant between the upper and lower substrates in an area near an edge of the upper substrate;

a plurality of source and gate pads on the lower substrate;

a plurality of gate and data lines on the lower substrate, each gate line being electrically connected with the corresponding gate pad, each data line being electrically connected with the corresponding source pad;

a gate insulating layer between the gate lines and the data lines;

a source PCB and a gate PCB electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB; and

a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB, further comprising a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire.

6. (Previously Presented) A liquid crystal display device, comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a sealant between the upper and lower substrates;

a plurality of source and gate pads on the lower substrate;

a plurality of gate and data lines on the lower substrate, each gate line being electrically connected with the corresponding gate pad, each data line being electrically connected with the corresponding source pad;

a gate insulating layer between the gate lines and the data lines;

a source PCB electrically connected with the plurality of source pads;

a gate PCB electrically connected with the plurality of gate pads;

a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB; and

a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire, wherein a specific resistance of the repair wire is below 10μΩ/cm inclusive.

7. (Original) The device of claim 5, wherein the repair wire is positioned in a region defined by the sealant.

8. (Original) The device of claim 5, wherein the repair wire is positioned across the sealant.

9. (Previously Presented) A liquid crystal display device, comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a sealant between the upper and lower substrates;

a plurality of source and gate pads on the lower substrate;

a plurality of gate and data lines on the lower substrate, each gate line being electrically connected with the corresponding gate pad, each data line being electrically connected with the corresponding source pad;

a gate insulating layer between the gate lines and the data lines;

a source PCB electrically connected with the plurality of source pads;

a gate PCB electrically connected with the plurality of gate pads;

a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB; and

a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire, wherein the repair wire includes first and second closed roofs, the first closed roof being formed along first edge of the upper substrate, the second closed roof being formed along second edge of the upper substrate.

10. (Previously Presented) A liquid crystal display device comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a sealant between the upper and lower substrates in an area near an edge of the upper substrate;

a plurality of source and gate pads on the lower substrate;

a plurality of gate and data lines on the lower substrate, each gate line being electrically connected with the corresponding gate pad, each data line being electrically connected with the corresponding source pad;

a gate insulating layer between the gate lines and the data lines;

a source PCB and a gate PCB electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB;

a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB; and

a first and second repair wire, the first repair wire crossing with each of the source pads with the gate insulating layer interposed therebetween, the

second repair wire crossing with each of the gate pads with the gate insulating layer interposed therebetween.

11. (Original) The device of claim 10, wherein a specific resistance of the first and second repair wires is below 10μΩ/cm inclusive.

12. (Previously Presented) A liquid crystal display device comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a sealant between the upper and lower substrates in an area near an edge of the upper substrate;

a plurality of source and gate pads on the lower substrate;

a plurality of gate and data lines on the lower substrate, each gate line being electrically connected with the corresponding gate pad, each data line being electrically connected with the corresponding source pad;

a gate insulating layer between the gate lines and the data lines;

a source PCB and a gate PCB electrically connected with the plurality of source pads and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB;

a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB; and

first and second dummy patterns on the lower substrate, the first dummy pattern being positioned along a first edge of the upper substrate, the second dummy pattern being positioned along a second edge of the upper substrate, the each dummy pattern having at least the same height as the gate transmitting wire.

13. (Original) The device of claim 12, further comprising auxiliary dummy patterns over the first and second dummy patterns.

14. (Previously Presented) A method of fabricating a liquid crystal display device, the method comprising:

preparing first and second substrates;

forming a plurality of gate lines, gate pads, gate transmitting wires, and dummy patterns on the first substrate;

forming a gate insulating layer on the gate lines, gate pads, gate transmitting wires, and dummy patterns;

forming a plurality of data lines and data pads on the gate insulating layer;

forming a passivation layer on the data lines and the data pads;

forming a sealant on the first substrate, wherein the gate transmitting wires connect the gate pads to the source pads across the sealant in the vicinity of a corner of the first substrate, and wherein the gate transmitting wires are formed in a curved shape on the lower substrate from the gate pads to the source pads;

attaching the first and second substrates;

scribing and breaking the second substrate; and

forming a liquid crystal layer between the first and second substrates.

15. (Cancelled)